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L Number	Hits	Search Text	DB	Tim stamp
-	998	jtag	USPAT	2002/05/01 15:04
-	502	jtag and id$2	USPAT	2002/07/02 12:45
-	133	jtag and id$2 and (reconfigur$7 or confirgur$7)	USPAT	2002/05/01 15:06
-	123	jtag and id$2 and (reconfigur$7 or confirgur$7) and software	USPAT	2002/05/01 15:06
-	88	jtag and (device with id$2) and (reconfigur$7 or confirgur$7) and software	USPAT	2002/05/01 15:06
-	72190	boundary adj2 scan or test adj access adj port or tap	USPAT	2002/07/02 12:47
-	1870	(boundary adj2 scan or test adj access adj port or tap) same (id or identification or code)	USPAT	2002/07/02 12:48
-	1991	(boundary adj2 scan or test adj access adj port or tap) same (id or identification or code)	USPAT	2002/07/02 12:48
-	253	((boundary adj2 scan or test adj access adj port or tap) same (id or identification or code)) same voltage	USPAT	2002/07/02 12:48
-	9	(((boundary adj2 scan or test adj access adj port or tap) same (id or identification or code)) same voltage) same pin$2	USPAT	2002/07/02 15:25
-	1	(tap with ((multiple or plural) with device with id))	USPAT	2002/07/02 15:27
-	2	(tap same ((multiple or plural) with device with id))	USPAT	2002/07/02 15:28
-	2	((tap or jtag or (boundary adj3 scan)) same ((multiple or plural) with device with id))	USPAT	2002/07/02 15:29
-	215	(plural or multiple) with id with code	USPAT	2002/07/02 15:30
-	11	((plural or multiple) with id with code) and (jtag or tap)	USPAT	2002/07/02 15:31
-	446	716/4.ccls.	USPAT	2002/07/02 15:31
-	27	716/4.ccls. and (jtag or tap or (boundary adj3 scan))	USPAT	2002/07/03 08:28
-	106	716/$.ccls. and (jtag or tap or (boundary adj3 scan))	USPAT	2002/07/03 08:29
-	27	716/4.ccls. and (jtag or tap or (boundary adj3 scan))	USPAT	2002/07/03 08:29
-	79	(716/$.ccls. and (jtag or tap or (boundary adj3 scan))) not (716/4.ccls. and (jtag or tap or (boundary adj3 scan)))	USPAT	2002/07/03 08:30
-	78	((716/$.ccls. and (jtag or tap or (boundary adj3 scan))) not (716/4.ccls. and (jtag or tap or (boundary adj3 scan)))) and (multiple or plural or different or several)	USPAT	2002/07/03 08:32
-	35	((716/$.ccls. and (jtag or tap or (boundary adj3 scan))) not (716/4.ccls. and (jtag or tap or (boundary adj3 scan)))) and ((multiple or plural or different or several) with device)	USPAT	2002/07/03 10:31
-	5	jtag and ((select$3 with (id or identification)) with code)	USPAT	2002/07/03 11:02
-	626	((378/34) or (378/35)).CCLS.	USPAT	2002/07/08 06:50
-	2224	(430/5).CCLS.	USPAT	2002/07/08 06:50
-	598	(((378/34) or (378/35)).CCLS.) and (wafer or substrate)	USPAT	2002/07/08 06:51
-	1840	((430/5).CCLS.) and (wafer or substrate)	USPAT	2002/07/08 06:50
-	395	((430/5).CCLS.) and ((wafer or substrate) same ((master adj2 mask) or reticle))	USPAT	2002/07/08 07:30
-	69	(((378/34) or (378/35)).CCLS.) and ((wafer or substrate) same ((master adj2 mask) or reticle))	USPAT	2002/07/08 06:52
-	68	((430/5).CCLS.) and (((wafer or substrate) same ((master adj2 mask) or reticle)) same (blank or shot or shoot or shooting or target))	USPAT	2002/07/08 07:31
-	336	(716/1).CCLS.	USPAT	2002/07/09 14:31
-	447	(716/4).CCLS.	USPAT	2002/07/09 14:31
-	759	((716/1).CCLS.) ((716/4).CCLS.)	USPAT	2002/07/09 14:31
-	42	(((716/1).CCLS.) ((716/4).CCLS.)) and (jtag or tap or (test adj access adj port) or (boundary adj scan))	USPAT	2002/07/09 15:11
-	26	(jtag or tap or (boundary adj scan)) same id adj3 code	USPAT; EPO; JPO; DERWENT; IBM_TDB	2002/07/10 11:24

:VALID *TDB-ACC-N : NA8909262

**DISCLOSURE TITLE: Using a Portion of the Boundary Register As the
Identification Register**

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CROSS REFERENCE: 0018-8689-32-4A-262

DISCLOSURE TEXT:

- In a standard design-for-testability architecture based on the boundary scan methods they*Ù, a device identification (ID) register is included that, on instruction, is loaded with information regarding the component and is then scanned to serially transmit this component information to test equipment or an other external resource. The information is typically the identification of the manufacturer, the com *** SEE ORIGINAL DOCUMENT ***** ponent part numb r and engin ring chang lev l, and f r programmable**

d vic s,
th d vice id ntificati n. On applicati n of the register is t
asily distinguish manufactur rs f d vices n a mixed
te hn l gy
board (one where multiple component sources are used).
- A shift register latch (SRL) that is suitable for use as a
stage in the device identification register is shown in Fig. 1.
The
ID Code Bit input is hard-wired to a logical 0 or 1 level
depending
upon the value needed for the ID at that bit position in the
register. The ID Code Bits are loaded into the register by
CAPTURE
ID CLK, one pulse of which occurs when "Read Identification
Register"
is the instruction. Following this load, the register is scanned
out
using the SHIFT A and SHIFT B clocks.
- As defined in they*Ù, the device identification register is
a
separate register within the architecture. However, a portion
f the
boundary scan register can be used to implement the device
identification function, saving almost all the circuitry in the
original identification register.
- Fig. 2 shows the boundary scan register circuitry for a
component primary output pin. (The circuitry for an input pin
is
nearly identical.) When +Wire Test+0, the logic drives through
the
AND/OR gate combination to the output pin and to the SRL
(this mode
is used for internal testing). When +Wire Test=1, the value in
the
SRL drives through to the output pin (this mode is used for
xt rnal

r wire t sting). ***** SEE RIGINAL DOCUMENT *****

An SRL with tw data p rts is btainabl by adding on AND-
ext nd r gate t th SRL f Fig. 2. This SRL can n w be us d for
both the boundary scan and the device identification register.

- Fig. 3 shows the extended SRL in use in a portion of the boundary scan register (the extended SRL is used in only so much of the boundary scan register as is needed for the device ID).
- The two operations, scanning the boundary registers and scanning the ID register, are mutually exclusive so there is no interference between the two functions.
- What remains is to ensure that only the device identification portion of the boundary scan register is shifted during the "Read Identification Register" operation. This can be accomplished using a multiplexer, as shown in Fig. 4 so that only the Device ID portion of the boundary register is scanned during a Read ID operation.
- Reference: "A Test Access Port and Boundary Scan Architecture," Technical Sub-Committee of the Joint Test Action Group (JTAG), Version 2.0, 30 March 1988.

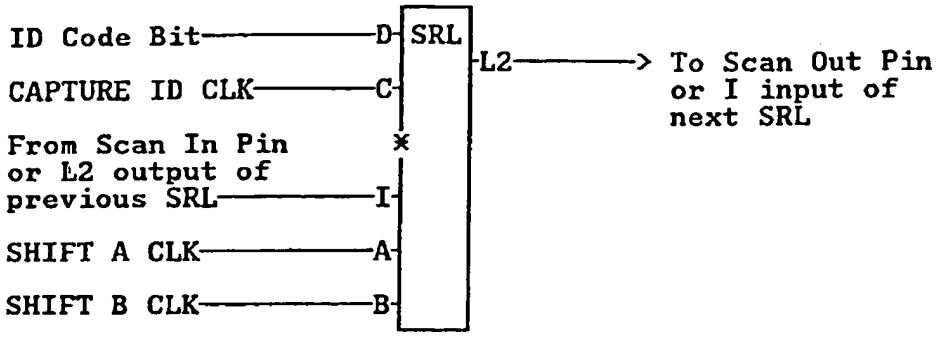

Figure 1.

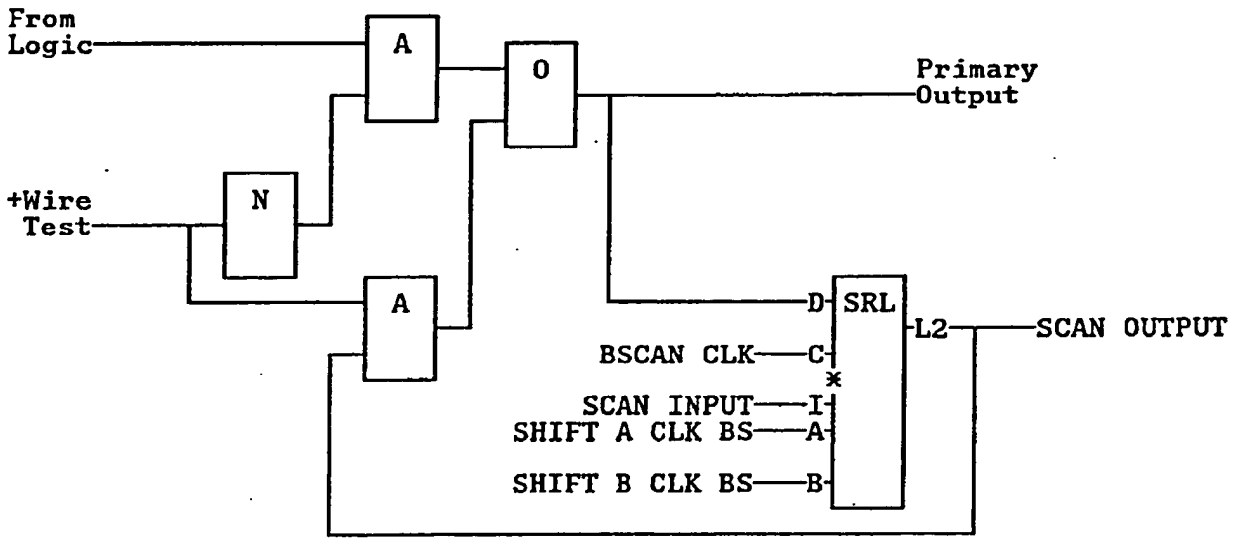

Figure 2.

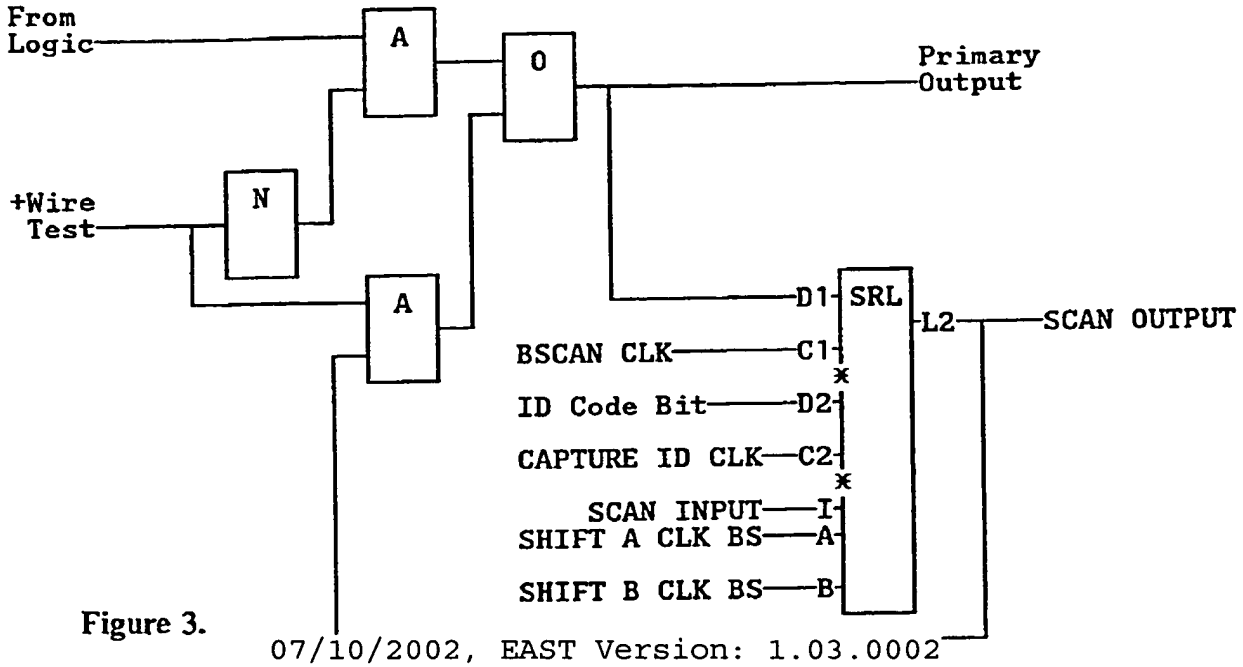

Figure 3.

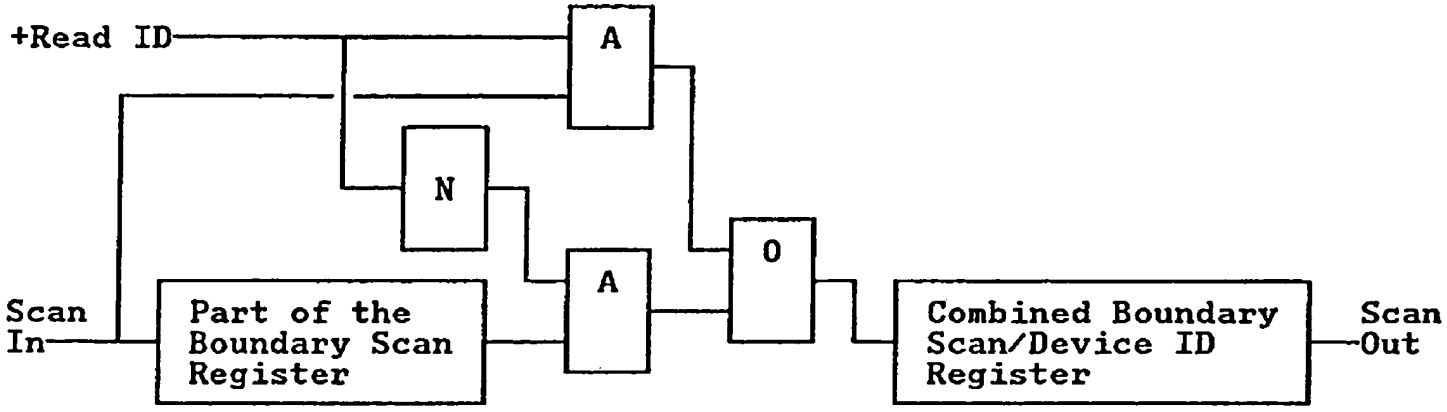
+Read ID
A
N
A
O
Scan In
Part of the Boundary Scan Register
Combined Boundary Scan/Device ID Register
Scan Out

Figure 4.